SIMLAB

REAL-TIME LAB PLATFORM FOR MATLAB/SIMULINK

Quick Reference

release 1.1

May 1, 2017

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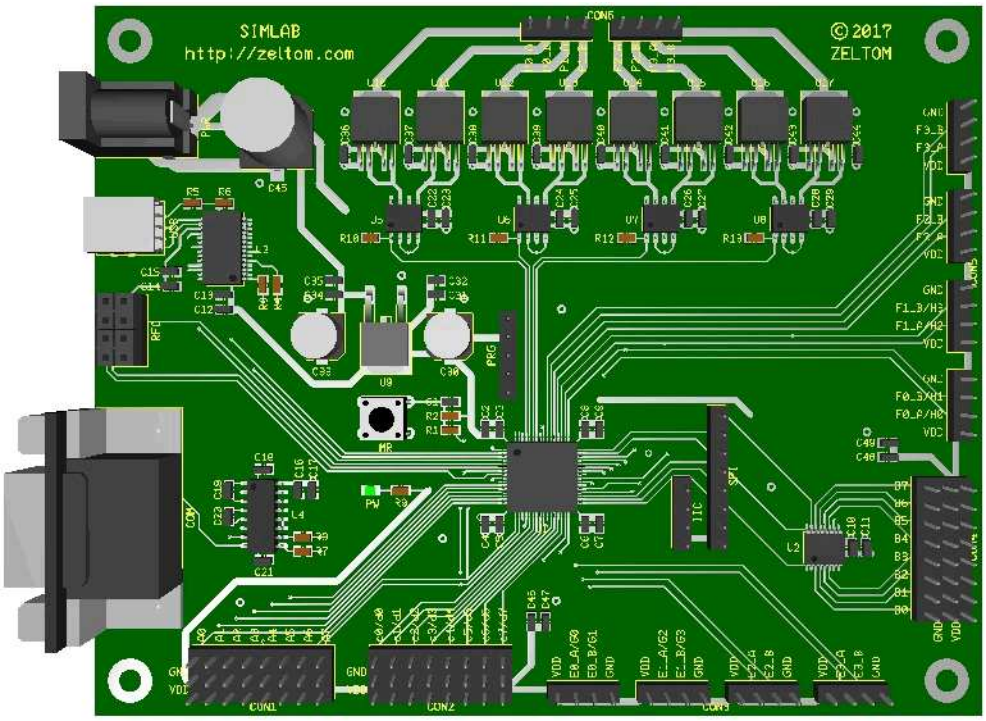
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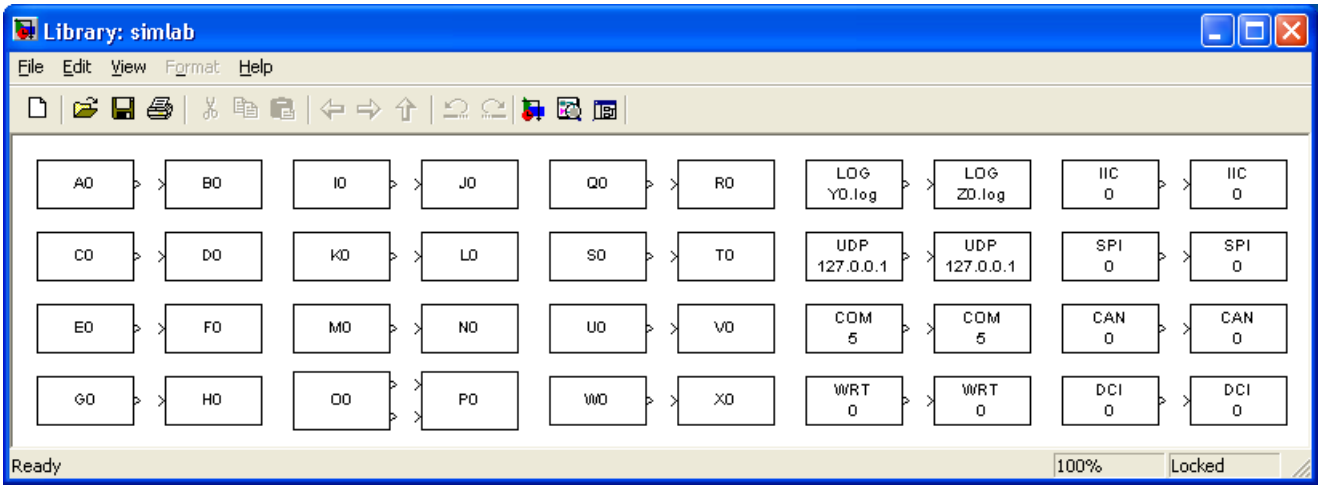
Library: simlab
File Edit View Format Help
A0 B0 I0 J0 Q0 R0 LOG Y0.log LOG Z0.log IIC 0 IIC 0
C0 D0 K0 L0 S0 T0 UDP 127.0.0.1 UDP 127.0.0.1 SPI 0 SPI 0
E0 F0 M0 N0 U0 V0 COM 5 COM 5 CAN 0 CAN 0
G0 H0 O0 P0 W0 X0 WRT 0 WRT 0 DCI 0 DCI 0
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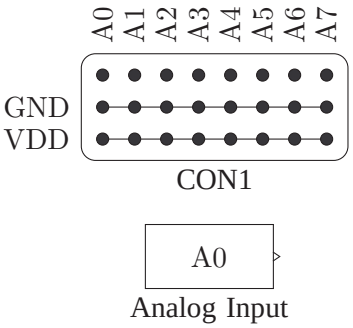
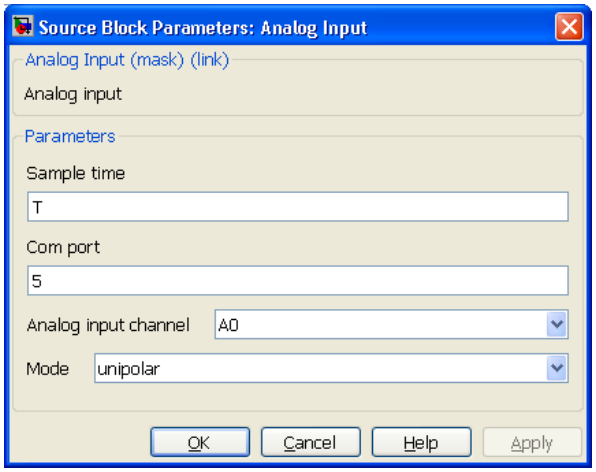
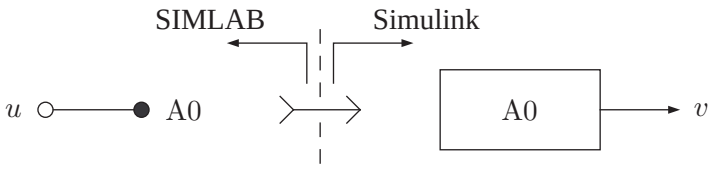
1. Analog Input

- 8 analog input channels $A0 - A7$
- Board input: $0 - 5$ V analog signal
- Block output: unipolar or bipolar amplitude of analog signal
- Resolution: 12 bit
- Sampling rate: 28.7891 kHz (internal)
- 610.3516 μV maximum unipolar amplitude quantization error and 1220.7031 μV maximum bipolar amplitude quantization error





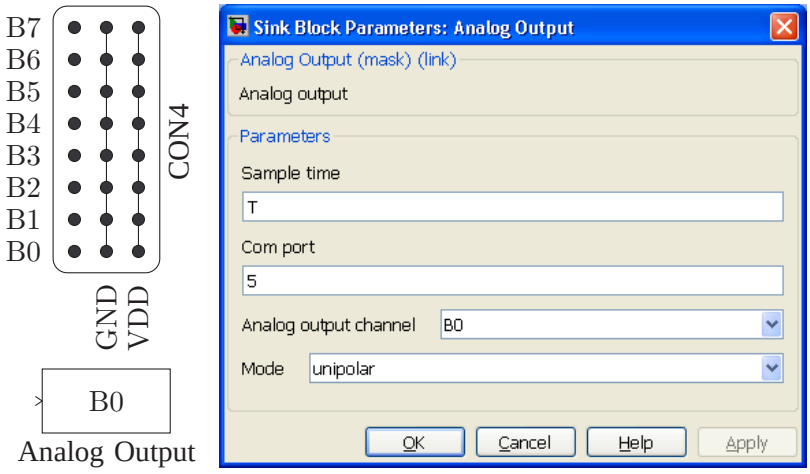


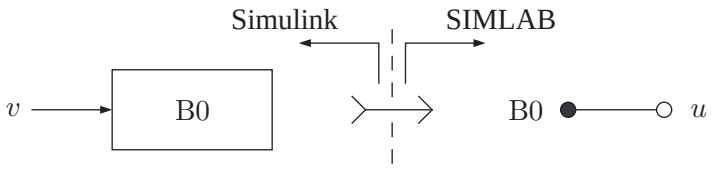
$$\text{unipolar mode} \quad \Rightarrow \quad v \approx \begin{cases} 5, & u \geq 5 \\ u, & 0 < u < 5 \\ 0, & u \leq 0 \end{cases}$$

$$\text{bipolar mode} \quad \Rightarrow \quad v \approx \begin{cases} +5, & u \geq 5 \\ 2u - 5, & 0 < u < 5 \\ -5, & u \leq 0 \end{cases}$$

2. Analog Output

- 8 analog output channels B0 – B7
- Block input: unipolar or bipolar amplitude of analog signal
- Board output: 0 – 5 V analog signal
- Resolution: 12 bit
- Settling time: 6.0 μs
- 610.3516 μV maximum unipolar amplitude interpolation error and 1220.7031 μV maximum bipolar amplitude interpolation error



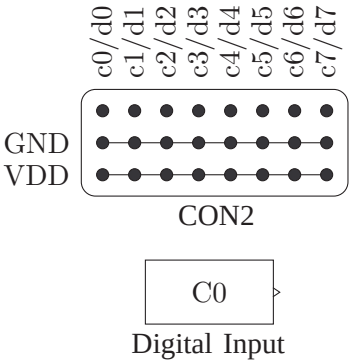


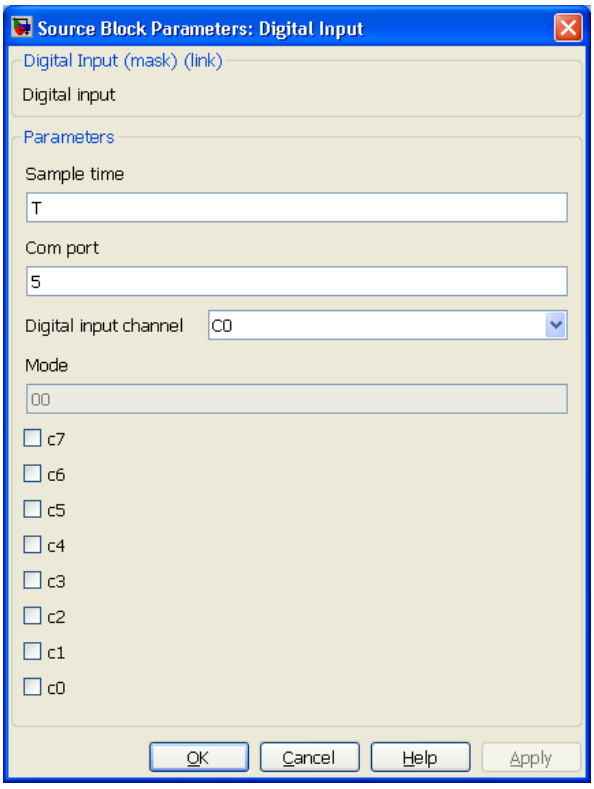
$$\text{unipolar mode} \quad \Rightarrow \quad u \approx \begin{cases} 5, & v \geq 5 \\ v, & 0 < v < 5 \\ 0, & v \leq 0 \end{cases}$$

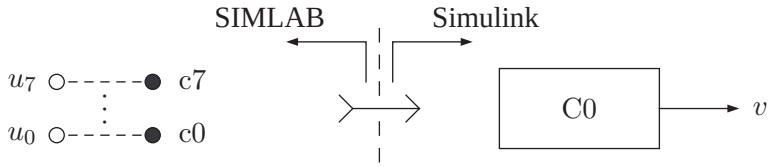
$$\text{bipolar mode} \quad \Rightarrow \quad u \approx \begin{cases} 5, & v \geq +5 \\ v/2 + 5/2, & -5 < v < +5 \\ 0, & v \leq -5 \end{cases}$$

3. Digital Input

- 1 digital input channel C0 with 8 digital input lines c0 – c7
- Board input: 0 – 5 V digital signal
- Block output: decimal representation of digital signal





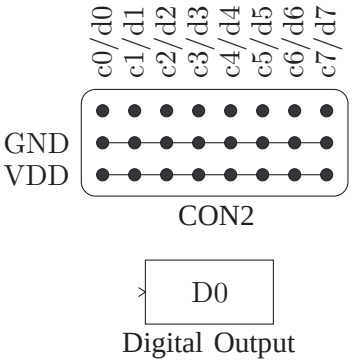


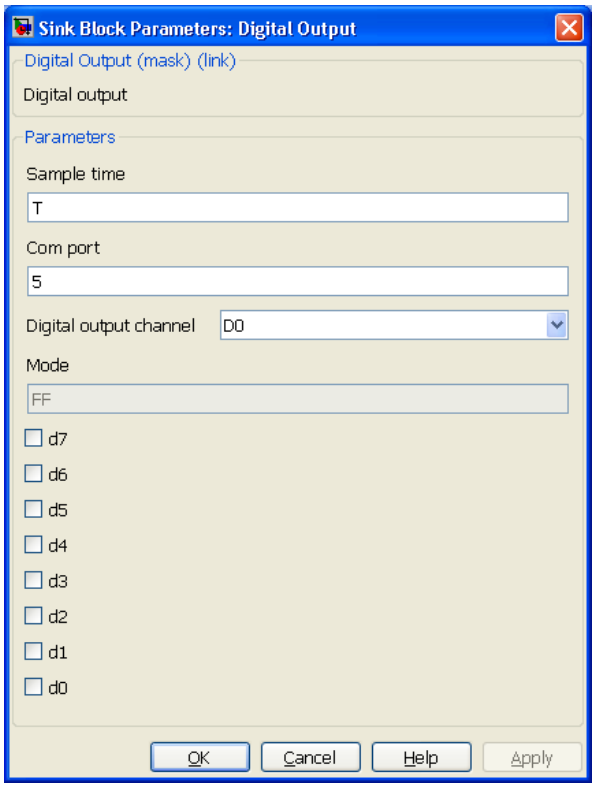
$$v = 128\,c_7 + 64\,c_6 + 32\,c_5 + 16\,c_4 + 8\,c_3 + 4\,c_2 + 2\,c_1 + 1\,c_0$$

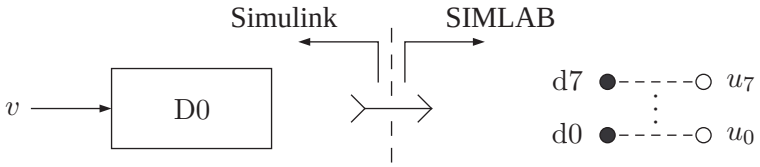
$$c_i = \begin{cases} u_i \text{ (1 or 0)}, & \text{ci is used (ci is checked)} \\ 0, & \text{ci and di are not used} \\ d_i \text{ (1 or 0)}, & \text{ci is not used and di is used with output } d_i \end{cases}$$

4. Digital Output

- 1 digital output channel D0 with 8 digital output lines d0 – d7
- Block input: decimal representation of digital signal
- Board output: 0 – 5 V digital signal





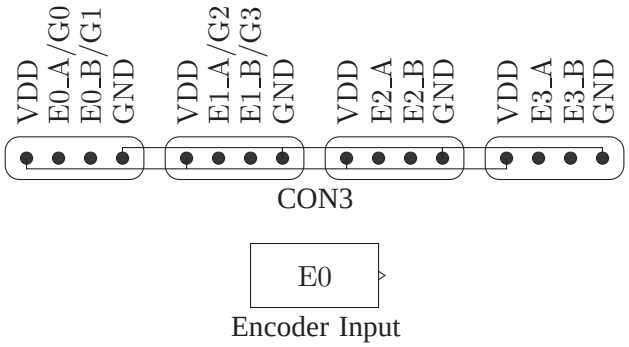


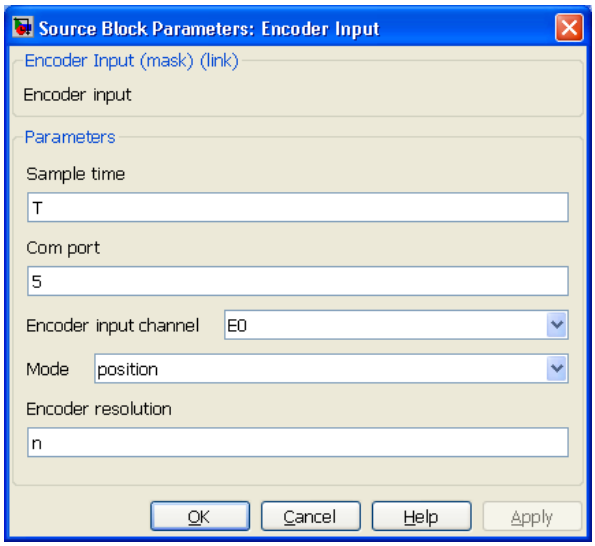
$$128\,d_7 + 64\,d_6 + 32\,d_5 + 16\,d_4 + 8\,d_3 + 4\,d_2 + 2\,d_1 + 1\,d_0 = v \;\&\; 0 \times 00\text{FF}$$

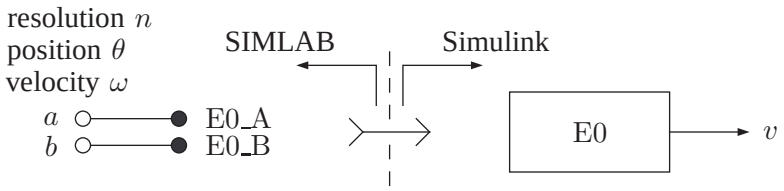
$$u_i = \begin{cases} d_i \text{ (1 or 0)}, & \text{ci is not used and di is used (di is checked)} \\ 0, & \text{ci and di are not used} \\ c_i \text{ (1 or 0)}, & \text{ci is used with input } c_i \end{cases}$$

5. Encoder Input

- 4 encoder input channels E0 – E3 with quadrature inputs E0_A, E0_B – E3_A, E3_B
- Board input: 0 – 5 V digital encoder signals
- Block output: position or velocity of encoder
- Resolution: 16 bit per sampling interval
- Scan rate: 307.0833 kHz
- $\pi/2/n$ rad maximum position quantization error and $153541.6667\,\pi/n$ rad/s maximum measurable angular speed (n is the encoder resolution)





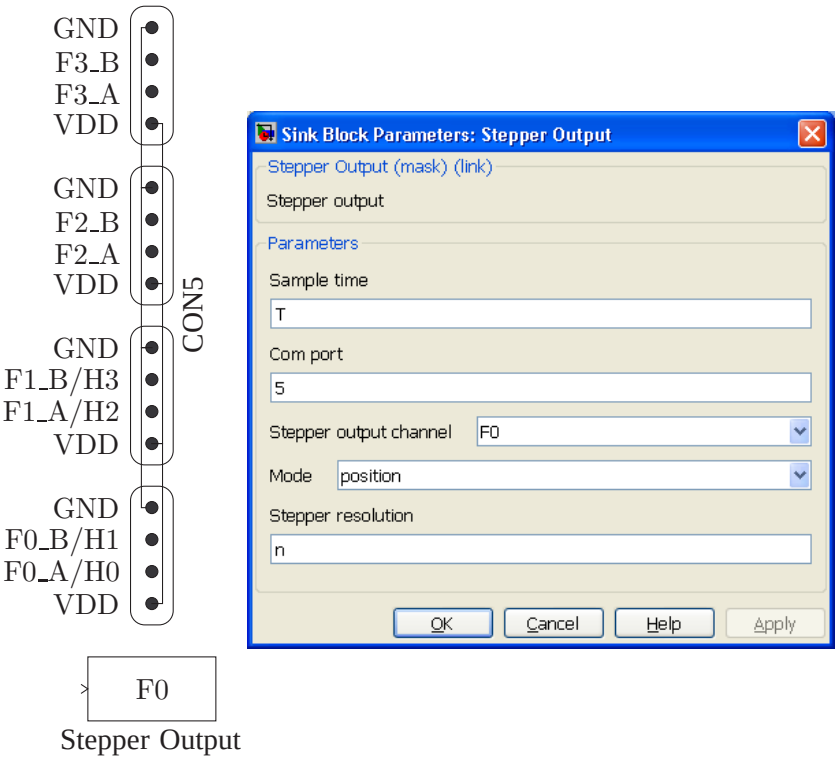


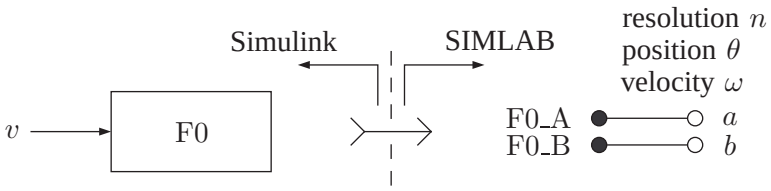
position mode $\Rightarrow$ $v \approx \theta$

velocity mode $\Rightarrow$ $v \approx \omega$

6. Stepper Output

- 4 stepper output channel $\mathrm{F0} - \mathrm{F3}$ with quadrature outputs F0_A, F0_B – F3_A, F3_B
- Block input: position or velocity of stepper
- Board output: $0 - 5$ V digital stepper signals
- Resolution: 16 bit per sampling interval
- Update rate: 28.7891 kHz
- $\pi/2/n$ rad maximum position interpolation error and $899.6582\,\pi/n$ rad/s maximum achievable angular speed (n is the stepper resolution)



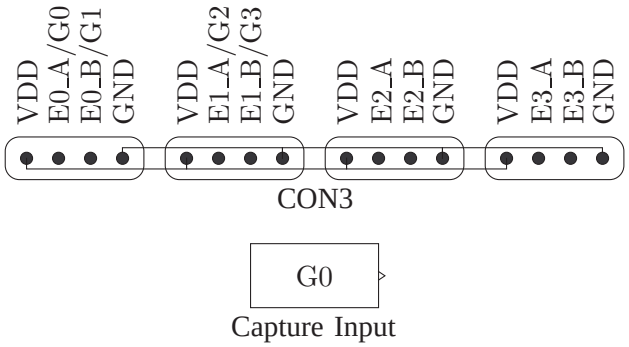


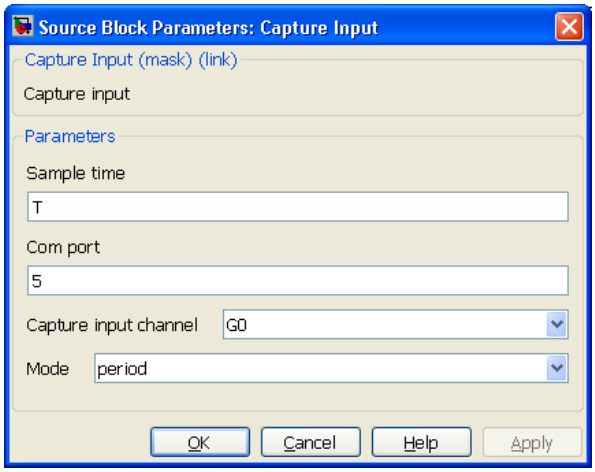
position mode $\Rightarrow$ $\theta \approx v$

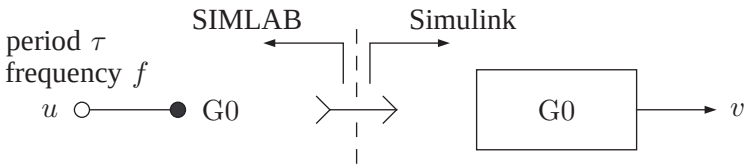
velocity mode $\Rightarrow$ $\omega \approx v$

7. Capture Input

- 4 capture input channels $G0 - G3$
- Board input: $0 - 5$ V digital signal
- Block output: period or frequency of digital signal
- Resolution: 16 bit
- Accuracy: 2.1710 μs
- 2.1710 μs maximum period quantization error and $f - 460625/\lfloor 460625/f \rfloor$ Hz maximum frequency quantization error (f is the actual input frequency)





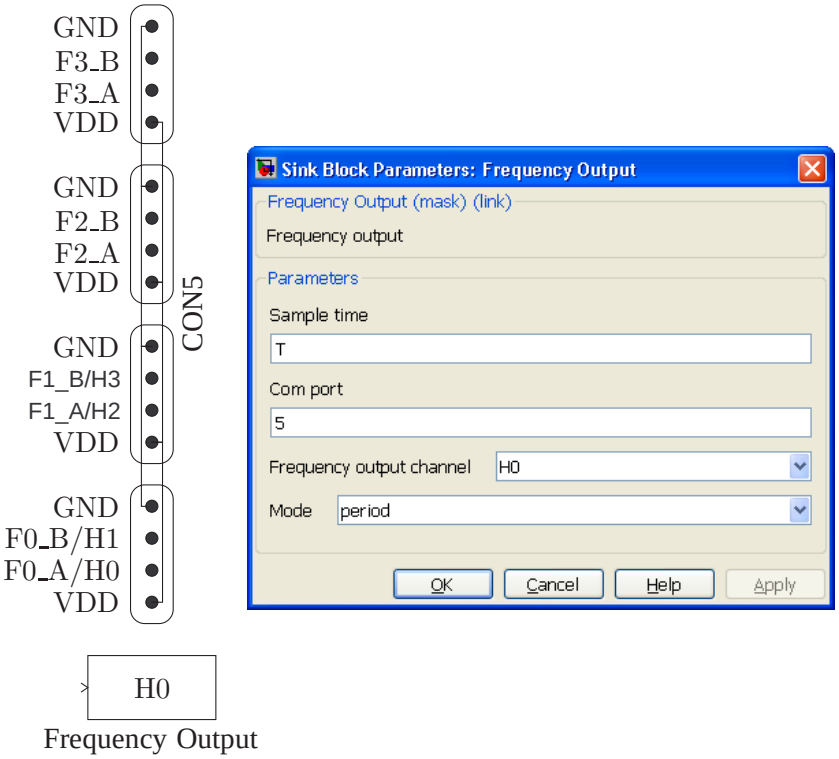


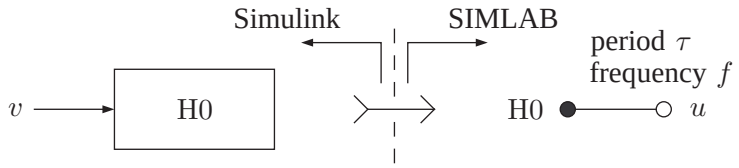
$$\text{period mode} \quad \Rightarrow \quad v \approx \begin{cases} 142.2763 \times 10^{-3}, & \tau \geq 142.2763 \times 10^{-3} \\ \tau, & 34.7354 \times 10^{-6} < \tau < 142.2763 \times 10^{-3} \\ 34.7354 \times 10^{-6}, & \tau \leq 34.7354 \times 10^{-6} \end{cases}$$

$$\text{frequency mode} \quad \Rightarrow \quad v \approx \begin{cases} 28789.0625, & f \geq 28789.0625 \\ f, & 7.0286 < f < 28789.0625 \\ 7.0286, & f \leq 7.0286 \end{cases}$$

8. Frequency Output

- 4 frequency output channels $\mathrm{H0} - \mathrm{H3}$
- Block input: period or frequency of digital signal
- Board output: $0 - 5$ V digital signal
- Resolution: 16 bit
- Accuracy: 2.1710 μs
- 2.1710 μs maximum period interpolation error and $f - 460625/\lfloor 460625/f \rfloor$ Hz maximum frequency interpolation error (f is the desired output frequency)



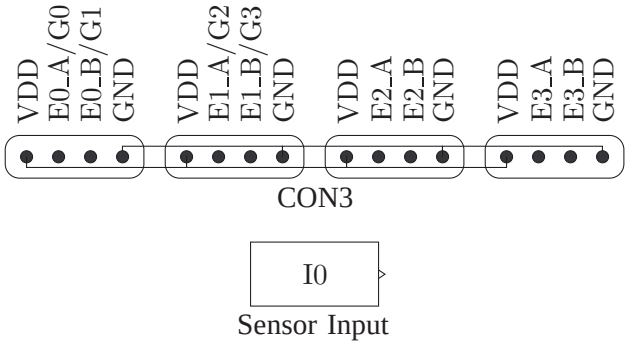


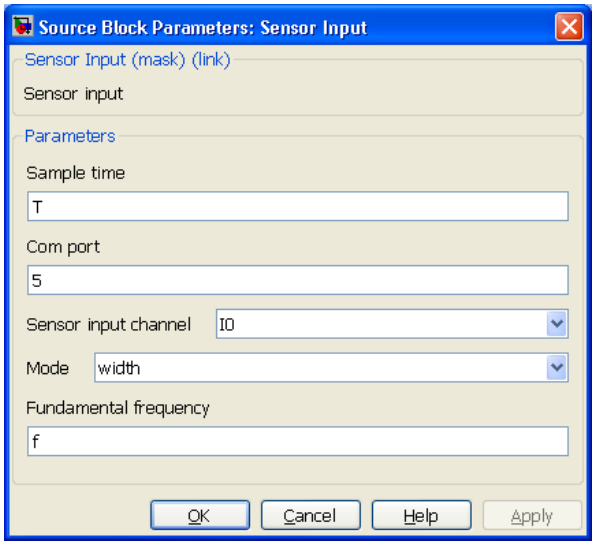
$$\text{period mode} \quad \Rightarrow \quad \tau \approx \begin{cases} 142.2763 \times 10^{-3}, & v \geq 142.2763 \times 10^{-3} \\ v, & 34.7354 \times 10^{-6} < v < 142.2763 \times 10^{-3} \\ 34.7354 \times 10^{-6}, & v \leq 34.7354 \times 10^{-6} \end{cases}$$

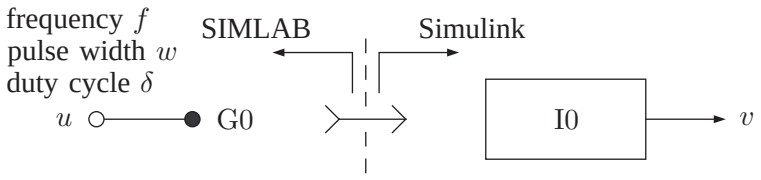
$$\text{frequency mode} \quad \Rightarrow \quad f \approx \begin{cases} 28789.0625, & v \geq 28789.0625 \\ v, & 7.0286 < v < 28789.0625 \\ 7.0286, & v \leq 7.0286 \end{cases}$$

9. Sensor Input

- 4 sensor input channels $\mathrm{I0} - \mathrm{I3}$
- Board input: $0 - 5$ V digital signal
- Block output: pulse width or duty cycle of digital signal
- Resolution: 16 bit
- Frequency range: $7.0286 \text{ Hz} \leq f \leq 1799.3164 \text{ Hz}$
- 2.1710 μs maximum pulse width quantization error and $2.1710 \times 10^{-6} f$ maximum duty cycle quantization error (f is the actual input frequency)





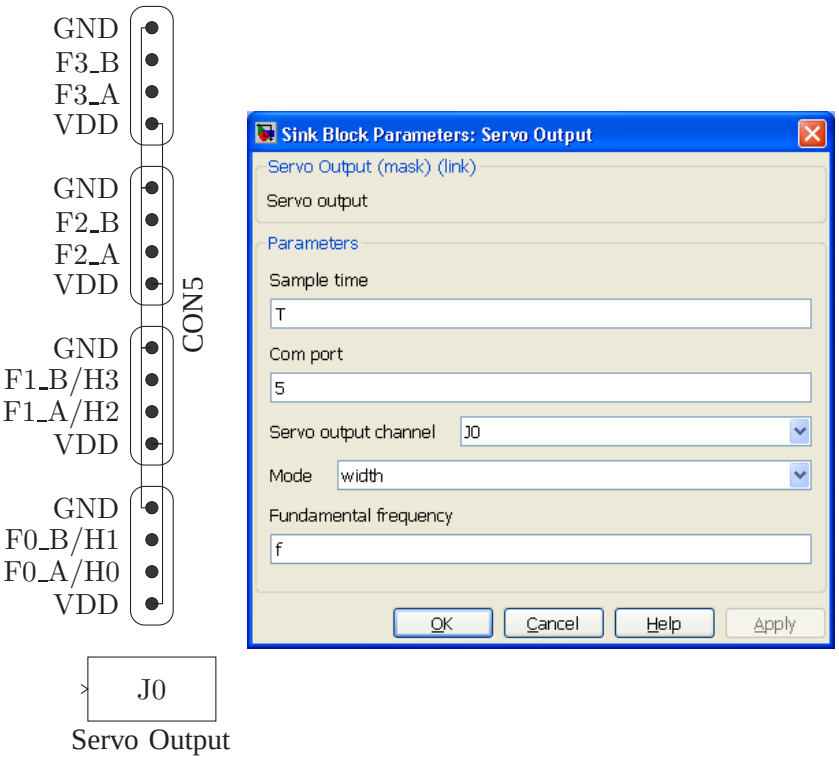


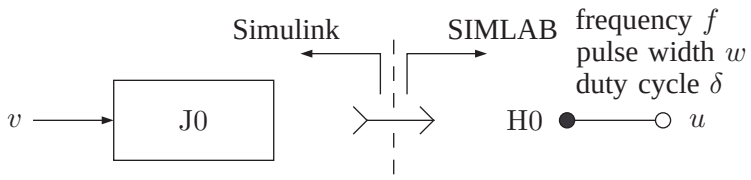
$$\text{width mode} \quad \Rightarrow \quad v \approx \begin{cases} 1/f - 34.7354 \times 10^{-6}, & w \geq 1/f - 34.7354 \times 10^{-6} \\ w, & 34.7354 \times 10^{-6} < w < 1/f - 34.7354 \times 10^{-6} \\ 34.7354 \times 10^{-6}, & w \leq 34.7354 \times 10^{-6} \end{cases}$$

$$\text{duty mode} \quad \Rightarrow \quad v \approx \begin{cases} 1 - 34.7354 \times 10^{-6} f, & \delta \geq 1 - 34.7354 \times 10^{-6} f \\ \delta, & 34.7354 \times 10^{-6} f < \delta < 1 - 34.7354 \times 10^{-6} f \\ 34.7354 \times 10^{-6} f, & \delta \leq 34.7354 \times 10^{-6} f \end{cases}$$

10. Servo Output

- 4 servo output channels $\mathrm{J0}-\mathrm{J3}$
- Block input: pulse width or duty cycle of digital signal
- Board output: $0-5$ V digital signal
- Resolution: 16 bit
- Frequency range: $7.0286 \text{ Hz} \leq f \leq 1799.3164 \text{ Hz}$
- 2.1710 μs maximum pulse width interpolation error and $2.1710 \times 10^{-6} f$ maximum duty cycle interpolation error (f is the desired output frequency)



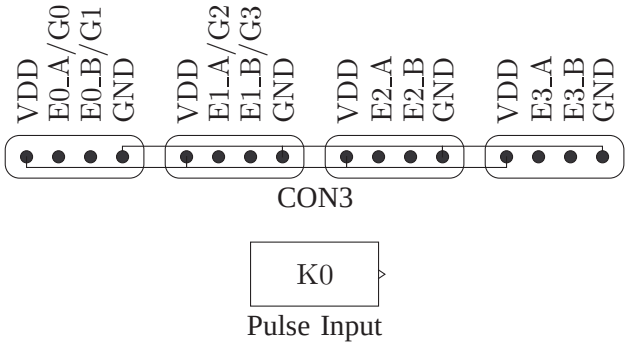


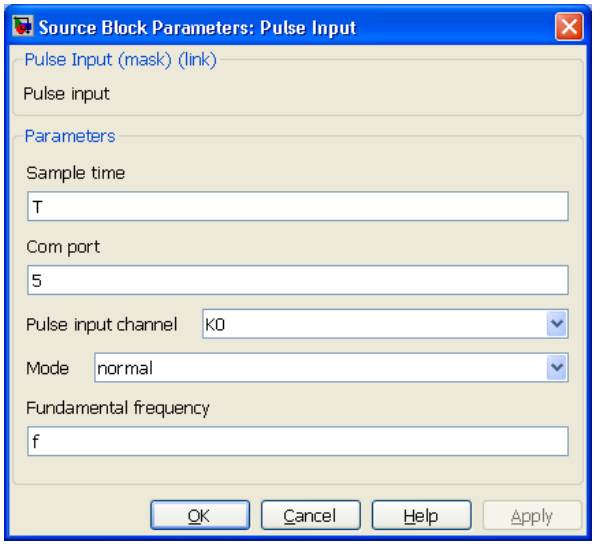
$$\text{width mode} \quad \Rightarrow \quad w \approx \begin{cases} 1/f - 34.7354 \times 10^{-6}, & v \geq 1/f - 34.7354 \times 10^{-6} \\ v, & 34.7354 \times 10^{-6} < v < 1/f - 34.7354 \times 10^{-6} \\ 34.7354 \times 10^{-6}, & v \leq 34.7354 \times 10^{-6} \end{cases}$$

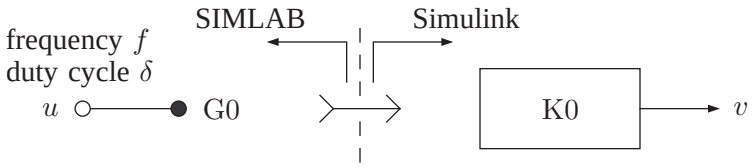
$$\text{duty mode} \quad \Rightarrow \quad \delta \approx \begin{cases} 1 - 34.7354 \times 10^{-6} f, & v \geq 1 - 34.7354 \times 10^{-6} f \\ v, & 34.7354 \times 10^{-6} f < v < 1 - 34.7354 \times 10^{-6} f \\ 34.7354 \times 10^{-6} f, & v \leq 34.7354 \times 10^{-6} f \end{cases}$$

11. Pulse Input

- 4 pulse input channels $\mathrm{K0}-\mathrm{K3}$
- Board input: $0-5$ V digital signal
- Block output: normal or shifted duty cycle of digital signal
- Resolution: 16 bit
- Frequency range: $56.2286 \text{ Hz} \leq f \leq 14394.5313 \text{ Hz}$
- $271.3704 \times 10^{-9} f$ maximum normal duty cycle quantization error and $542.7408 \times 10^{-9} f$ maximum shifted duty cycle quantization error (f is the actual input frequency)





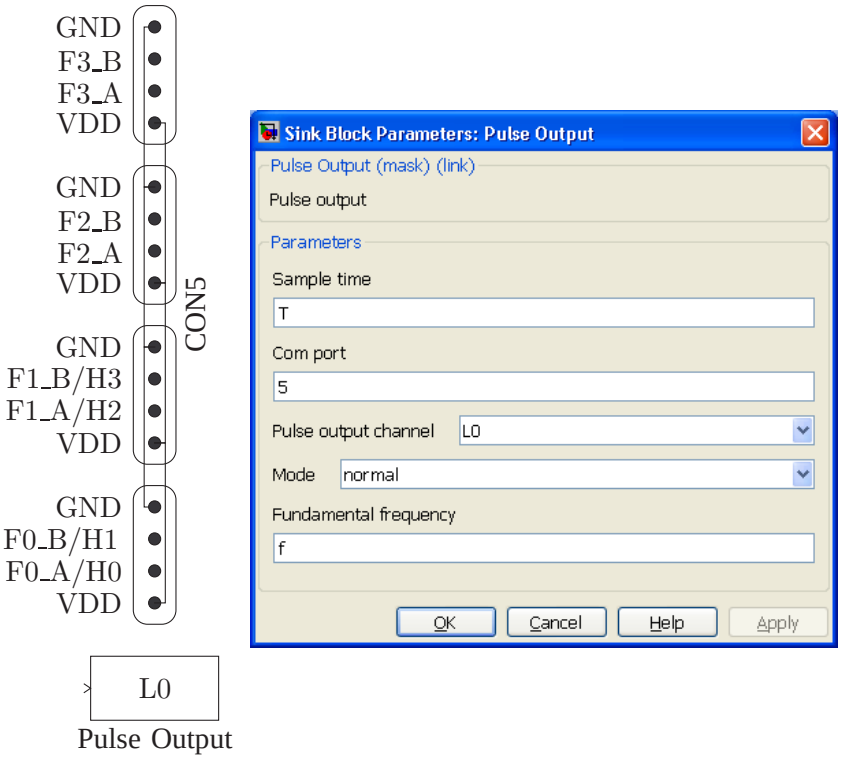


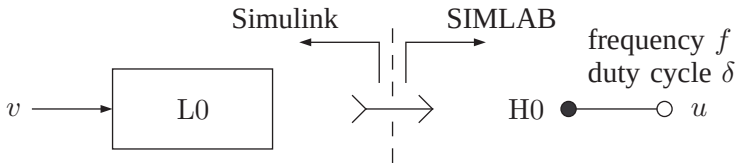
$$\text{duty mode} \quad \Rightarrow \quad v \approx \begin{cases} 1 - 4.3419 \times 10^{-6} f, & \delta \geq 1 - 4.3419 \times 10^{-6} f \\ \delta, & 4.3419 \times 10^{-6} f < \delta < 1 - 4.3419 \times 10^{-6} f \\ 4.3419 \times 10^{-6} f, & \delta \leq 4.3419 \times 10^{-6} f \end{cases}$$

$$\text{shifted mode} \quad \Rightarrow \quad v \approx \begin{cases} +1 - 8.6839 \times 10^{-6} f, & \delta \geq 1 - 4.3419 \times 10^{-6} f \\ 2\delta - 1, & 4.3419 \times 10^{-6} f < \delta < 1 - 4.3419 \times 10^{-6} f \\ -1 + 8.6839 \times 10^{-6} f, & \delta \leq 4.3419 \times 10^{-6} f \end{cases}$$

12. Pulse Output

- 4 pulse output channels $\mathrm{L0}-\mathrm{L3}$
- Block input: normal or shifted duty cycle of digital signal
- Board output: $0-5$ V digital signal
- Resolution: 16 bit
- Frequency range: $56.2286\ \mathrm{Hz} \leq f \leq 14394.5313\ \mathrm{Hz}$
- $271.3704\times10^{-9}f$ maximum normal duty cycle interpolation error and $542.7408\times10^{-9}f$ maximum shifted duty cycle interpolation error (f is the desired output frequency)



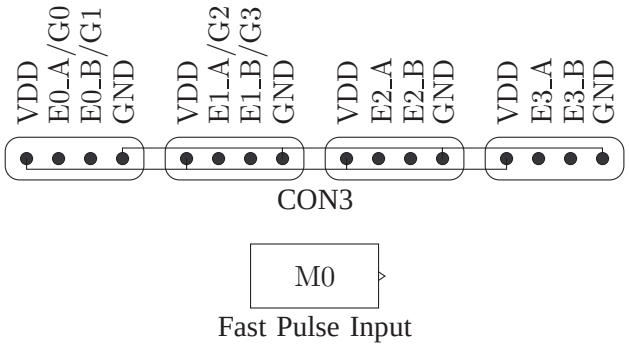


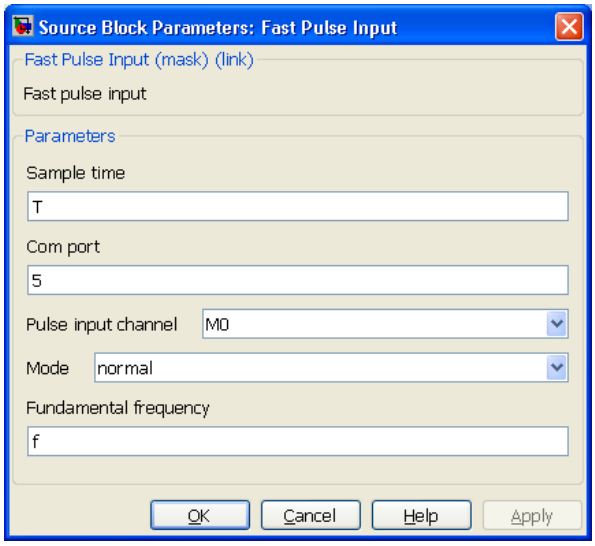
$$\text{duty mode} \quad \Rightarrow \quad \delta \approx \begin{cases} 1-4.3419\times10^{-6}f, & v \geq 1-4.3419\times10^{-6}f \\ v, & 4.3419\times10^{-6}f < v < 1-4.3419\times10^{-6}f \\ 4.3419\times10^{-6}f, & v \leq 4.3419\times10^{-6}f \end{cases}$$

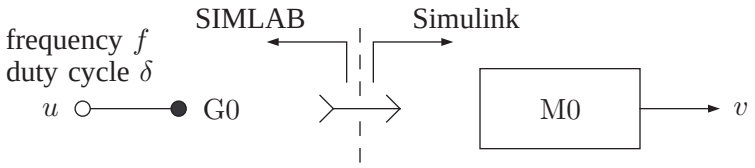
$$\text{shifted mode} \quad \Rightarrow \quad \delta \approx \begin{cases} 1-4.3419\times10^{-6}f, & v \geq +1-8.6839\times10^{-6}f \\ v/2+1/2, & -1+8.6839\times10^{-6}f < v < +1-8.6839\times10^{-6}f \\ 4.3419\times10^{-6}f, & v \leq -1+8.6839\times10^{-6}f \end{cases}$$

13. Fast Pulse Input

- 4 fast pulse input channels $\mathrm{M0}-\mathrm{M3}$
- Board input: $0-5$ V digital signal
- Block output: normal or shifted duty cycle of digital signal
- Resolution: 16 bit
- Frequency range: $449.8291 \text{ Hz} \leq f \leq 115156.25 \text{ Hz}$
- $33.9213 \times 10^{-9} f$ maximum normal duty cycle quantization error and $67.8426 \times 10^{-9} f$ maximum shifted duty cycle quantization error (f is the actual input frequency)





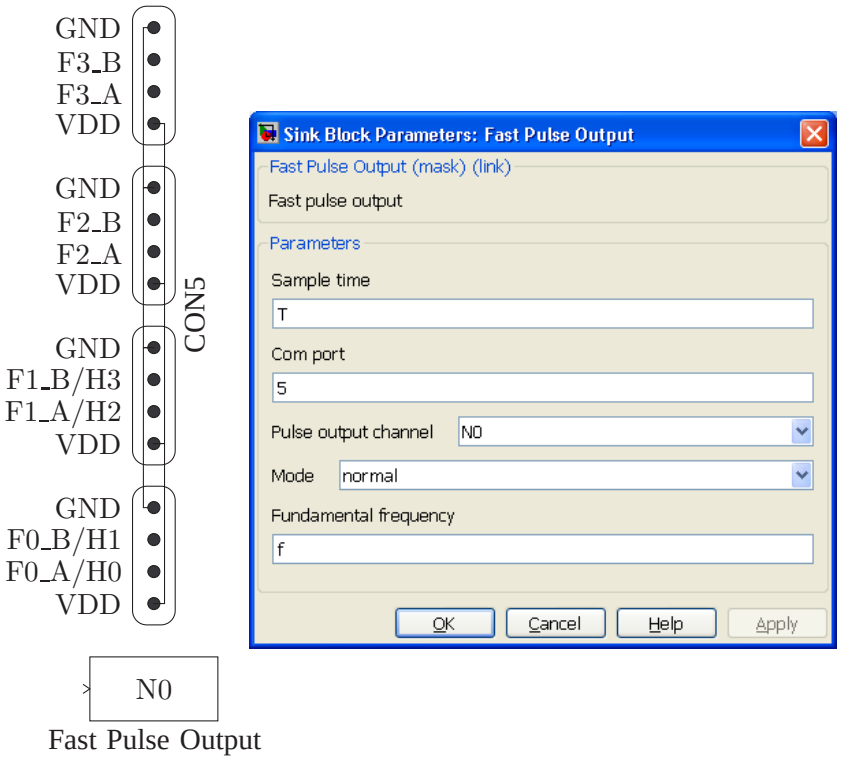


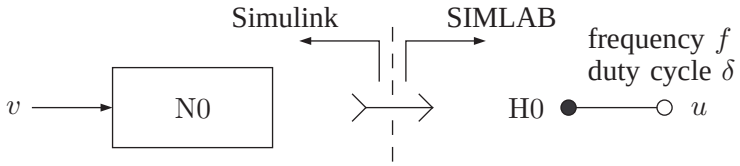
$$\text{normal mode} \quad \Rightarrow \quad v \approx \begin{cases} 1, & \delta \geq 1 \ (u \text{ is high}) \\ \delta, & 0 < \delta < 1 \\ 0, & \delta \leq 0 \ (u \text{ is low}) \end{cases}$$

$$\text{shifted mode} \quad \Rightarrow \quad v \approx \begin{cases} +1, & \delta \geq 1 \ (u \text{ is high}) \\ 2\delta - 1, & 0 < \delta < 1 \\ -1, & \delta \leq 0 \ (u \text{ is low}) \end{cases}$$

14. Fast Pulse Output

- 4 fast pulse output channels $\mathrm{N0} - \mathrm{N3}$
- Block input: normal or shifted duty cycle of digital signal
- Board output: $0 - 5$ V digital signal
- Resolution: 16 bit
- Frequency range: $449.8291 \text{ Hz} \leq f \leq 115156.25 \text{ Hz}$
- $33.9213 \times 10^{-9} f$ maximum normal duty cycle interpolation error and $67.8426 \times 10^{-9} f$ maximum shifted duty cycle interpolation error (f is the desired output frequency)



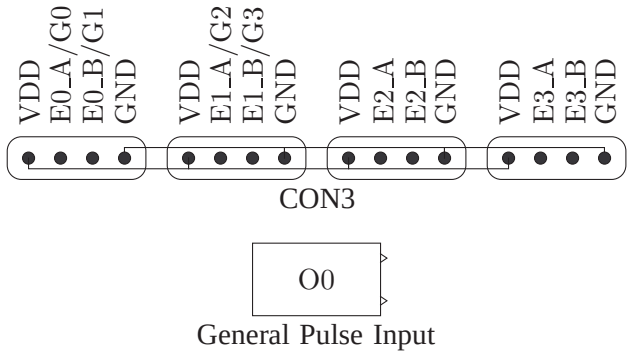


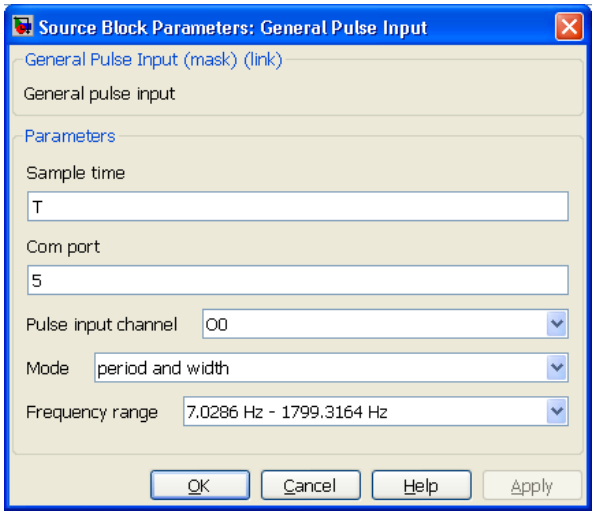
$$\text{normal mode} \quad \Rightarrow \quad \delta \approx \begin{cases} 1 \ (u \text{ is high}), & v \geq 1 \\ v, & 0 < v < 1 \\ 0 \ (u \text{ is low}), & v \leq 0 \end{cases}$$

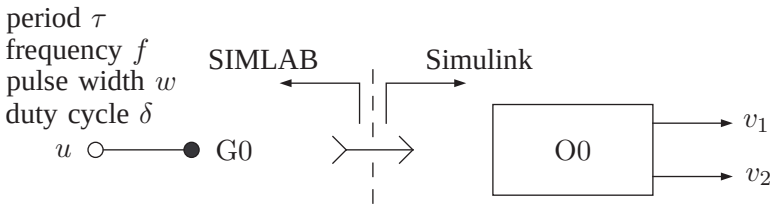
$$\text{shifted mode} \quad \Rightarrow \quad \delta \approx \begin{cases} 1 \ (u \text{ is high}), & v \geq +1 \\ v/2 + 1/2, & -1 < v < +1 \\ 0 \ (u \text{ is low}), & v \leq -1 \end{cases}$$

15. General Pulse Input

- 4 general pulse input channels $\mathrm{O0} - \mathrm{O3}$
- Board input: $0 - 5$ V digital signal
- Block output: period or frequency and pulse width or duty cycle of digital signal
- Resolution: 16 bit
- Frequency range: $7.0286 \text{ Hz} \leq f \leq 1799.3164 \text{ Hz}$ or $56.2286 \text{ Hz} \leq f \leq 14394.5313 \text{ Hz}$
- 2.1710 μs or 271.3704 ns maximum period quantization error and $f - 460625/\lfloor 460625/f \rfloor$ Hz or $f - 3685000/\lfloor 3685000/f \rfloor$ Hz maximum frequency quantization error (f is the actual input frequency)
- 2.1710 μs or 271.3704 ns maximum pulse width quantization error and $2.1710 \times 10^{-6} f$ or $271.3704 \times 10^{-9} f$ maximum duty cycle quantization error (f is the actual input frequency)







period and width mode $\Rightarrow$

$$v_1 \approx \begin{cases} 142.2763 \times 10^{-3}/\kappa, & \tau \geq 142.2763 \times 10^{-3}/\kappa \\ \tau, & 555.7666 \times 10^{-6}/\kappa < \tau < 142.2763 \times 10^{-3}/\kappa \\ 555.7666 \times 10^{-6}/\kappa, & \tau \leq 555.7666 \times 10^{-6}/\kappa \end{cases}$$

$$v_2 \approx \begin{cases} 1/f - 34.7354 \times 10^{-6}/\kappa, & w \geq 1/f - 34.7354 \times 10^{-6}/\kappa \\ w, & 34.7354 \times 10^{-6}/\kappa < w < 1/f - 34.7354 \times 10^{-6}/\kappa \\ 34.7354 \times 10^{-6}/\kappa, & w \leq 34.7354 \times 10^{-6}/\kappa \end{cases}$$

period and duty mode $\Rightarrow$

$$v_1 \approx \begin{cases} 142.2763 \times 10^{-3}/\kappa, & \tau \geq 142.2763 \times 10^{-3}/\kappa \\ \tau, & 555.7666 \times 10^{-6}/\kappa < \tau < 142.2763 \times 10^{-3}/\kappa \\ 555.7666 \times 10^{-6}/\kappa, & \tau \leq 555.7666 \times 10^{-6}/\kappa \end{cases}$$

$$v_2 \approx \begin{cases} 1 - 34.7354 \times 10^{-6} f/\kappa, & \delta \geq 1 - 34.7354 \times 10^{-6} f/\kappa \\ \delta, & 34.7354 \times 10^{-6} f/\kappa < \delta < 1 - 34.7354 \times 10^{-6} f/\kappa \\ 34.7354 \times 10^{-6} f/\kappa, & \delta \leq 34.7354 \times 10^{-6} f/\kappa \end{cases}$$

frequency and width mode $\Rightarrow$

$$v_1 \approx \begin{cases} 1799.3164\kappa, & f \geq 1799.3164\kappa \\ f, & 7.0286\kappa < f < 1799.3164\kappa \\ 7.0286\kappa, & f \leq 7.0286\kappa \end{cases}$$

$$v_2 \approx \begin{cases} 1/f - 34.7354 \times 10^{-6}/\kappa, & w \geq 1/f - 34.7354 \times 10^{-6}/\kappa \\ w, & 34.7354 \times 10^{-6}/\kappa < w < 1/f - 34.7354 \times 10^{-6}/\kappa \\ 34.7354 \times 10^{-6}/\kappa, & w \leq 34.7354 \times 10^{-6}/\kappa \end{cases}$$

frequency and duty mode $\Rightarrow$

$$v_1 \approx \begin{cases} 1799.3164\kappa, & f \geq 1799.3164\kappa \\ f, & 7.0286\kappa < f < 1799.3164\kappa \\ 7.0286\kappa, & f \leq 7.0286\kappa \end{cases}$$

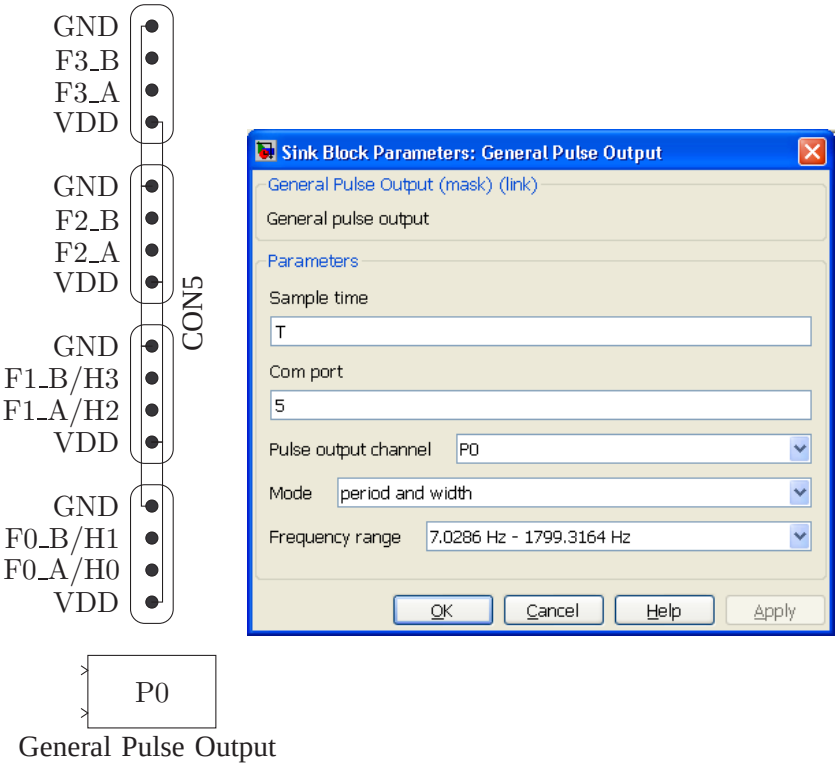
$$v_2 \approx \begin{cases} 1 - 34.7354 \times 10^{-6} f/\kappa, & \delta \geq 1 - 34.7354 \times 10^{-6} f/\kappa \\ \delta, & 34.7354 \times 10^{-6} f/\kappa < \delta < 1 - 34.7354 \times 10^{-6} f/\kappa \\ 34.7354 \times 10^{-6} f/\kappa, & \delta \leq 34.7354 \times 10^{-6} f/\kappa \end{cases}$$

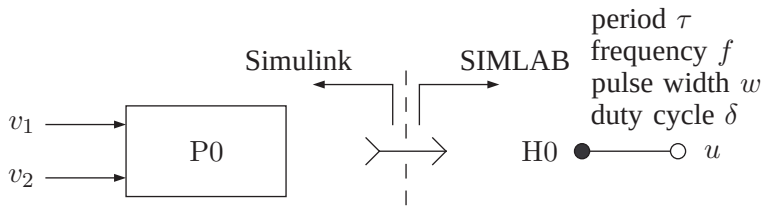
$\kappa = 1$ when 7.0286 Hz $-$ 1799.3164 Hz frequency range selected

$\kappa = 8$ when 56.2286 Hz $-$ 14394.5313 Hz frequency range selected

16. General Pulse Output

- 4 general pulse output channels $\mathrm{P0} - \mathrm{P3}$
- Block input: period or frequency and pulse width or duty cycle of digital signal
- Board output: $0 - 5$ V digital signal
- Resolution: 16 bit
- Frequency range: $7.0286 \text{ Hz} \leq f \leq 1799.3164 \text{ Hz}$ or $56.2286 \text{ Hz} \leq f \leq 14394.5313 \text{ Hz}$
- 2.1710 μs or 271.3704 ns maximum period interpolation error and $f - 460625/\lfloor 460625/f \rfloor$ Hz or $f - 3685000/\lfloor 3685000/f \rfloor$ Hz maximum frequency interpolation error (f is the desired output frequency)
- 2.1710 μs or 271.3704 ns maximum pulse width interpolation error and $2.1710 \times 10^{-6} f$ or $271.3704 \times 10^{-9} f$ maximum duty cycle interpolation error (f is the desired output frequency)





period and width mode $\Rightarrow$

$$\tau \approx \begin{cases} 142.2763 \times 10^{-3}/\kappa, & v_1 \geq 142.2763 \times 10^{-3}/\kappa \\ v_1, & 555.7666 \times 10^{-6}/\kappa < v_1 < 142.2763 \times 10^{-3}/\kappa \\ 555.7666 \times 10^{-6}/\kappa, & v_1 \leq 555.7666 \times 10^{-6}/\kappa \end{cases}$$

$$w \approx \begin{cases} 1/f - 34.7354 \times 10^{-6}/\kappa, & v_2 \geq 1/f - 34.7354 \times 10^{-6}/\kappa \\ v_2, & 34.7354 \times 10^{-6}/\kappa < v_2 < 1/f - 34.7354 \times 10^{-6}/\kappa \\ 34.7354 \times 10^{-6}/\kappa, & v_2 \leq 34.7354 \times 10^{-6}/\kappa \end{cases}$$

period and duty mode $\Rightarrow$

$$\tau \approx \begin{cases} 142.2763 \times 10^{-3}/\kappa, & v_1 \geq 142.2763 \times 10^{-3}/\kappa \\ v_1, & 555.7666 \times 10^{-6}/\kappa < v_1 < 142.2763 \times 10^{-3}/\kappa \\ 555.7666 \times 10^{-6}/\kappa, & v_1 \leq 555.7666 \times 10^{-6}/\kappa \end{cases}$$

$$\delta \approx \begin{cases} 1 - 34.7354 \times 10^{-6} f/\kappa, & v_2 \geq 1 - 34.7354 \times 10^{-6} f/\kappa \\ v_2, & 34.7354 \times 10^{-6} f/\kappa < v_2 < 1 - 34.7354 \times 10^{-6} f/\kappa \\ 34.7354 \times 10^{-6} f/\kappa, & v_2 \leq 34.7354 \times 10^{-6} f/\kappa \end{cases}$$

frequency and width mode $\Rightarrow$

$$f \approx \begin{cases} 1799.3164\kappa, & v_1 \geq 1799.3164\kappa \\ v_1, & 7.0286\kappa < v_1 < 1799.3164\kappa \\ 7.0286\kappa, & v_1 \leq 7.0286\kappa \end{cases}$$

$$w \approx \begin{cases} 1/f - 34.7354 \times 10^{-6}/\kappa, & v_2 \geq 1/f - 34.7354 \times 10^{-6}/\kappa \\ v_2, & 34.7354 \times 10^{-6}/\kappa < v_2 < 1/f - 34.7354 \times 10^{-6}/\kappa \\ 34.7354 \times 10^{-6}/\kappa, & v_2 \leq 34.7354 \times 10^{-6}/\kappa \end{cases}$$

frequency and duty mode $\Rightarrow$

$$f \approx \begin{cases} 1799.3164\kappa, & v_1 \geq 1799.3164\kappa \\ v_1, & 7.0286\kappa < v_1 < 1799.3164\kappa \\ 7.0286\kappa, & v_1 \leq 7.0286\kappa \end{cases}$$

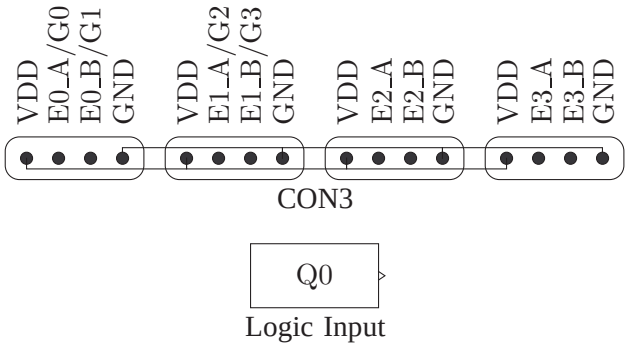
$$\delta \approx \begin{cases} 1 - 34.7354 \times 10^{-6} f/\kappa, & v_2 \geq 1 - 34.7354 \times 10^{-6} f/\kappa \\ v_2, & 34.7354 \times 10^{-6} f/\kappa < v_2 < 1 - 34.7354 \times 10^{-6} f/\kappa \\ 34.7354 \times 10^{-6} f/\kappa, & v_2 \leq 34.7354 \times 10^{-6} f/\kappa \end{cases}$$

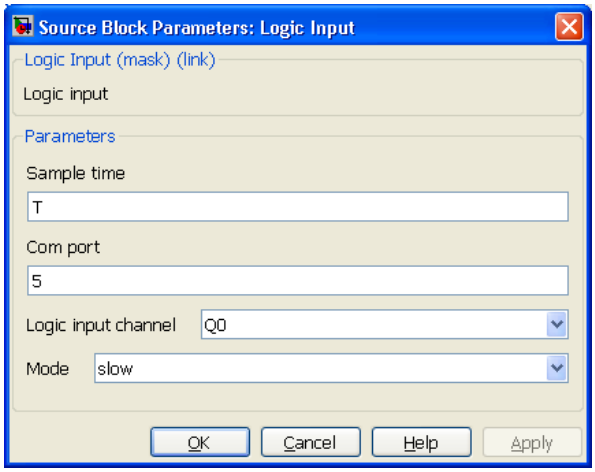
$\kappa = 1$ when 7.0286 Hz $-$ 1799.3164 Hz frequency range selected

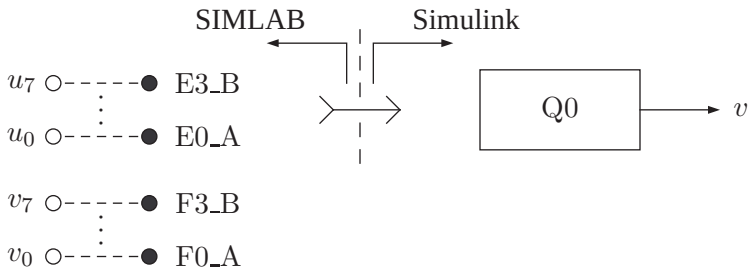
$\kappa = 8$ when 56.2286 Hz $-$ 14394.5313 Hz frequency range selected

17. Logic Input

- 1 logic input channel Q0 with 8 logic functions (or, nor, and, nand, exor, exnor, buffer, inverter)
- Board input: $0 - 5$ V digital signal
- Board output: $0 - 5$ V digital signal
- Block output: ignored
- Propagation delay: 4 μs in slow mode and 1 μs in fast mode







slow mode or fast mode $\Rightarrow$

$$v_0 = u_0 + u_1, \quad v_1 = \overline{u_0 + u_1}$$

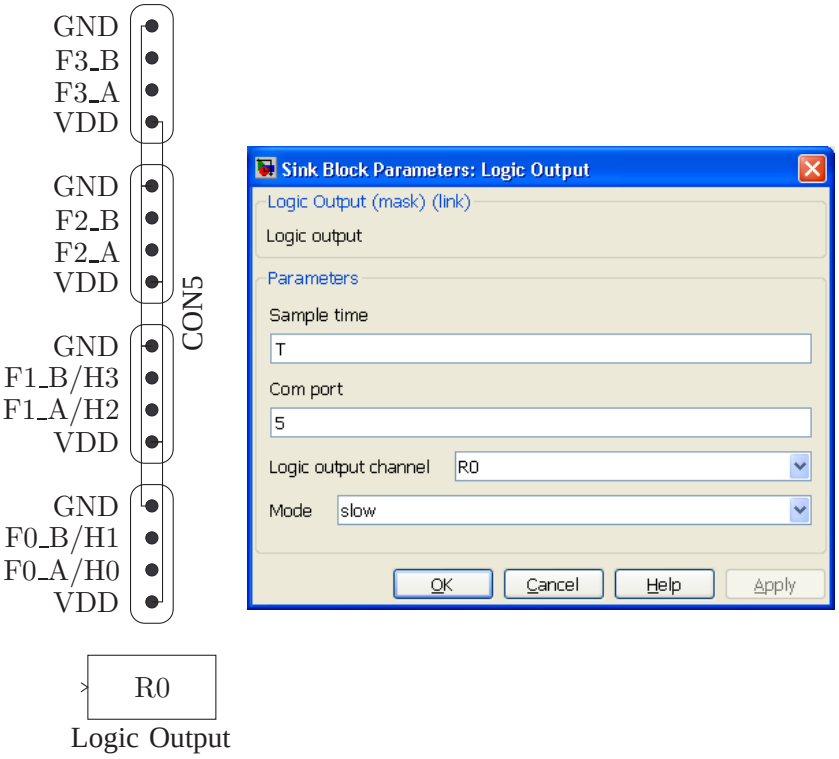
$$v_2 = u_2 \cdot u_3, \quad v_3 = \overline{u_2 \cdot u_3}$$

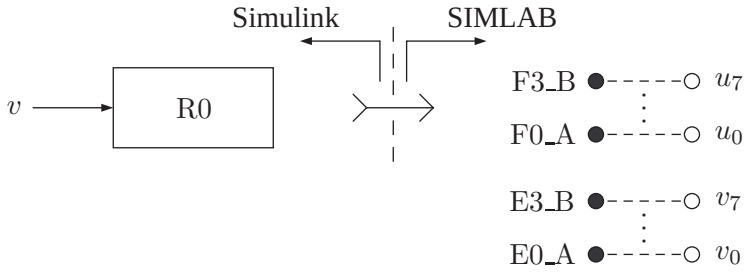
$$v_4 = u_4 \oplus u_5, \quad v_5 = u_4 \odot u_5$$

$$v_6 = u_6, \quad v_7 = \overline{u_7}$$

18. Logic Output

- 1 logic output channel R0 with 8 logic functions (or, nor, and, nand, exor, exnor, buffer, inverter)
- Block input: ignored
- Board input: $0 - 5$ V digital signal
- Board output: $0 - 5$ V digital signal
- Propagation delay: 4 μs in slow mode and 1 μs in fast mode





slow mode or fast mode $\Rightarrow$

$$u_0 = v_0 + v_1, \quad u_1 = \overline{v_0 + v_1}$$

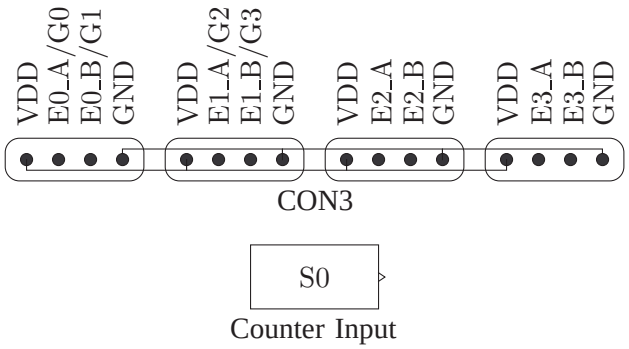
$$u_2 = v_2 \cdot v_3, \quad u_3 = \overline{v_2 \cdot v_3}$$

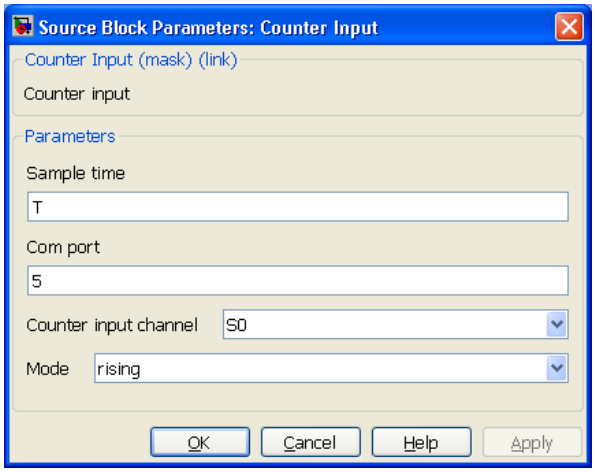
$$u_4 = v_4 \oplus v_5, \quad u_5 = v_4 \odot v_5$$

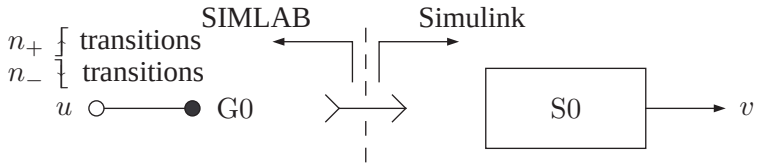
$$u_6 = v_6, \quad u_7 = \overline{v_7}$$

19. Counter Input

- 4 counter input channels $S0 - S3$
- Board input: $0 - 5$ V digital signal
- Block output: number of rising or falling edges of digital signal
- 16 bit register length and minimum 271.3704 ns separation





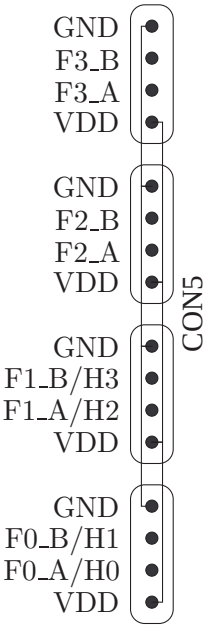


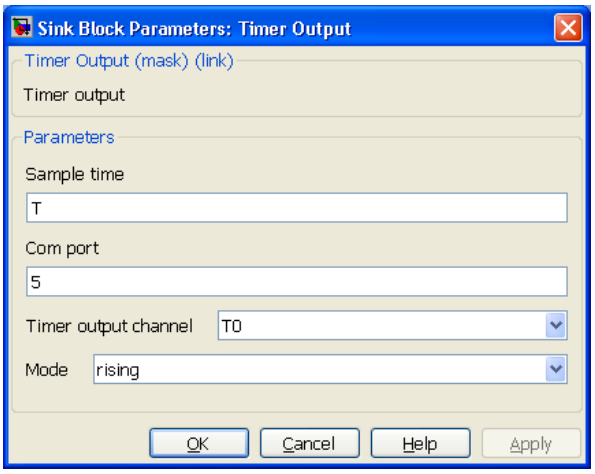
rising mode $\Rightarrow$ $v = n_+$

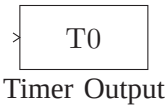
falling mode $\Rightarrow$ $v = n_-$

20. Timer Output

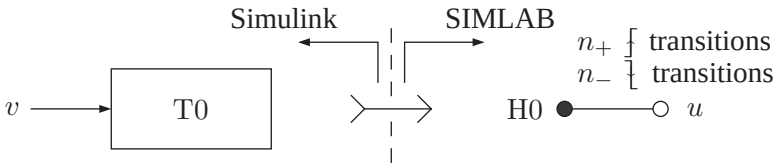
- 4 timer output channels $\mathrm{T0}-\mathrm{T3}$
- Block input: number of rising or falling edges of digital signal
- Board output: $0-5$ V digital signal
- 16 bit register length and 488.2972 μs separation







Timer Output

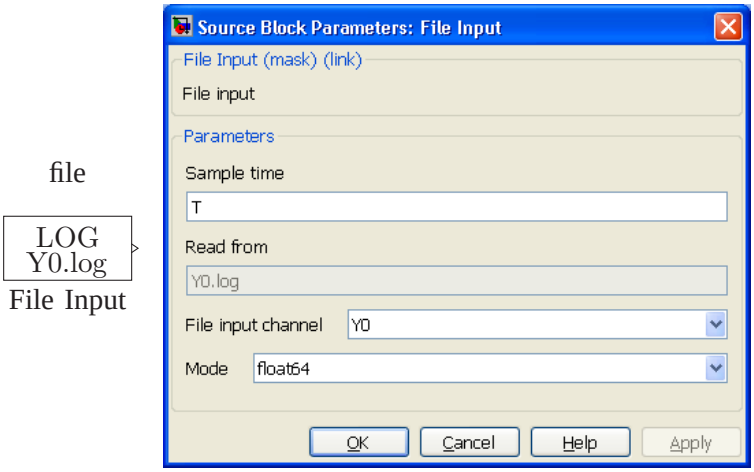


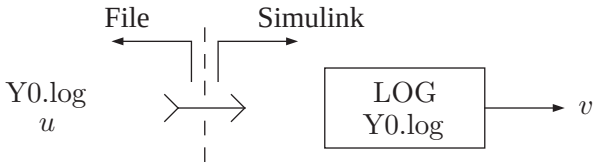
$$\text{rising mode} \quad \Rightarrow \quad n_+ = v$$

$$\text{falling mode} \quad \Rightarrow \quad n_- = v$$

21. File Input

- 16 file input channels LOG y.log (file name) with input file Y0.log – YF.log
- File input: data in float64, float32, int64, uint64, int32, uint32, int16, uint16, int8 or uint8 format
- Block output: data read from file input





float64 mode $\Rightarrow$ $v = \text{float64}(u)$

float32 mode $\Rightarrow$ $v = \text{float32}(u)$

int64 mode $\Rightarrow$ $v = \text{int64}(u)$

uint64 mode $\Rightarrow$ $v = \text{uint64}(u)$

int32 mode $\Rightarrow$ $v = \text{int32}(u)$

uint32 mode $\Rightarrow$ $v = \text{uint32}(u)$

int16 mode $\Rightarrow$ $v = \text{int16}(u)$

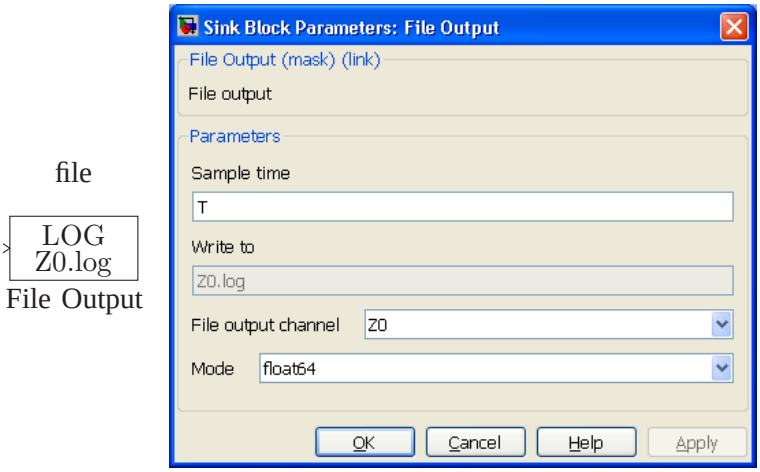
uint16 mode $\Rightarrow$ $v = \text{uint16}(u)$

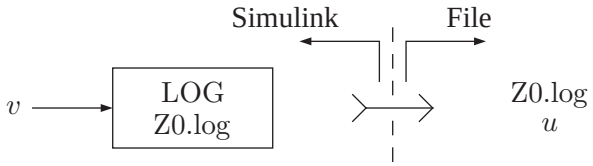
int8 mode $\Rightarrow$ $v = \text{int8}(u)$

uint8 mode $\Rightarrow$ $v = \text{uint8}(u)$

22. File Output

- 16 file output channels LOG z.log (file name) with output file Z0.log – ZF.log
- Block input: data to be written to file output
- File output: data in float64, float32, int64, uint64, int32, uint32, int16, uint16, int8 or uint8 format





float64 mode $\Rightarrow$ $u = \text{float64}(v)$

float32 mode $\Rightarrow$ $u = \text{float32}(v)$

int64 mode $\Rightarrow$ $u = \text{int64}(v)$

uint64 mode $\Rightarrow$ $u = \text{uint64}(v)$

int32 mode $\Rightarrow$ $u = \text{int32}(v)$

uint32 mode $\Rightarrow$ $u = \text{uint32}(v)$

int16 mode $\Rightarrow$ $u = \text{int16}(v)$

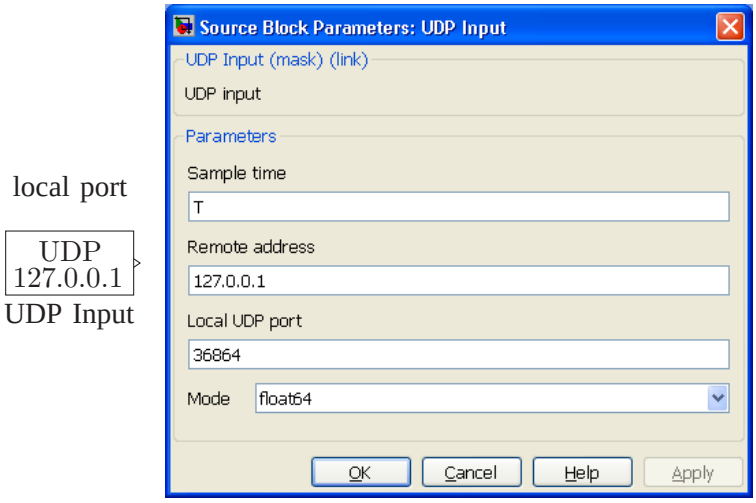
uint16 mode $\Rightarrow$ $u = \text{uint16}(v)$

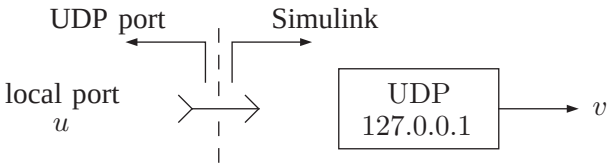
int8 mode $\Rightarrow$ $u = \text{int8}(v)$

uint8 mode $\Rightarrow$ $u = \text{uint8}(v)$

23. UDP Input

- 65536 UDP input channels UDP $y.y.y.y$ (IP address) with local port $0 - 65535$
- UDP input: data in float64, float32, int64, uint64, int32, uint32, int16, uint16, int8 or uint8 format
- Block output: data read from local port





float64 mode $\Rightarrow$ $v = \text{float64}(u)$

float32 mode $\Rightarrow$ $v = \text{float32}(u)$

int64 mode $\Rightarrow$ $v = \text{int64}(u)$

uint64 mode $\Rightarrow$ $v = \text{uint64}(u)$

int32 mode $\Rightarrow$ $v = \text{int32}(u)$

uint32 mode $\Rightarrow$ $v = \text{uint32}(u)$

int16 mode $\Rightarrow$ $v = \text{int16}(u)$

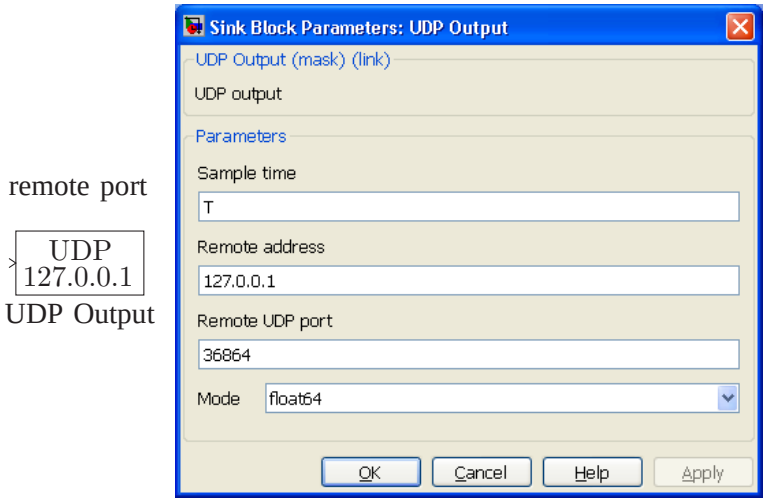
uint16 mode $\Rightarrow$ $v = \text{uint16}(u)$

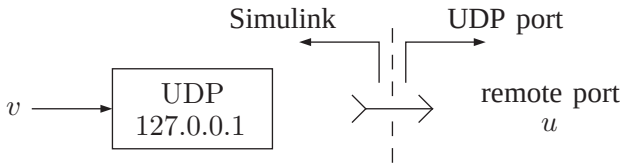
int8 mode $\Rightarrow$ $v = \text{int8}(u)$

uint8 mode $\Rightarrow$ $v = \text{uint8}(u)$

24. UDP Output

- 65536 UDP output channels UDP $z.z.z.z$ (IP address) with remote port $0 - 65535$
- Block input: data to be written to remote port
- UDP output: data in float64, float32, int64, uint64, int32, uint32, int16, uint16, int8 or uint8 format





float64 mode $\Rightarrow$ $u = \text{float64}(v)$

float32 mode $\Rightarrow$ $u = \text{float32}(v)$

int64 mode $\Rightarrow$ $u = \text{int64}(v)$

uint64 mode $\Rightarrow$ $u = \text{uint64}(v)$

int32 mode $\Rightarrow$ $u = \text{int32}(v)$

uint32 mode $\Rightarrow$ $u = \text{uint32}(v)$

int16 mode $\Rightarrow$ $u = \text{int16}(v)$

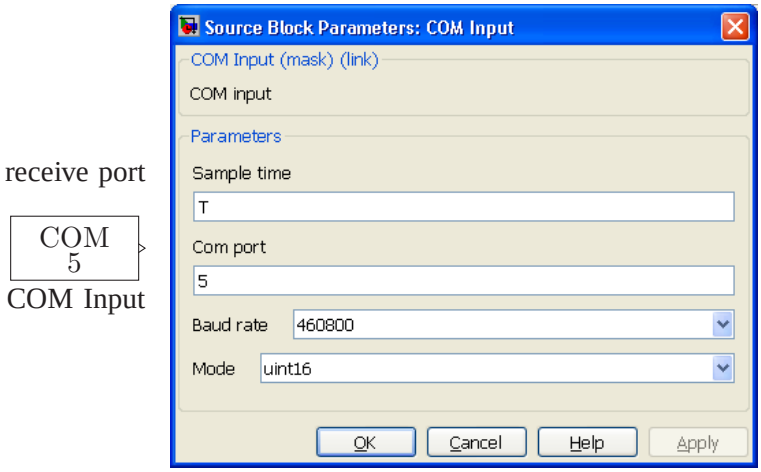
uint16 mode $\Rightarrow$ $u = \text{uint16}(v)$

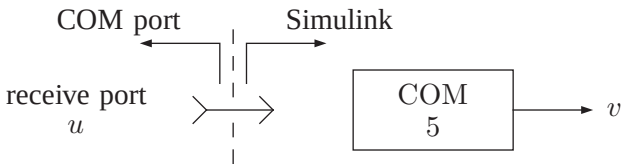
int8 mode $\Rightarrow$ $u = \text{int8}(v)$

uint8 mode $\Rightarrow$ $u = \text{uint8}(v)$

25. COM Input

- 256 COM input channels COM y (COM port) with receive port $1 - 256$
- COM input: data in float64, float32, int64, uint64, int32, uint32, int16, uint16, int8 or uint8 format
- Block output: data read from receive port





float64 mode $\Rightarrow$ $v = \text{float64}(u)$

float32 mode $\Rightarrow$ $v = \text{float32}(u)$

int64 mode $\Rightarrow$ $v = \text{int64}(u)$

uint64 mode $\Rightarrow$ $v = \text{uint64}(u)$

int32 mode $\Rightarrow$ $v = \text{int32}(u)$

uint32 mode $\Rightarrow$ $v = \text{uint32}(u)$

int16 mode $\Rightarrow$ $v = \text{int16}(u)$

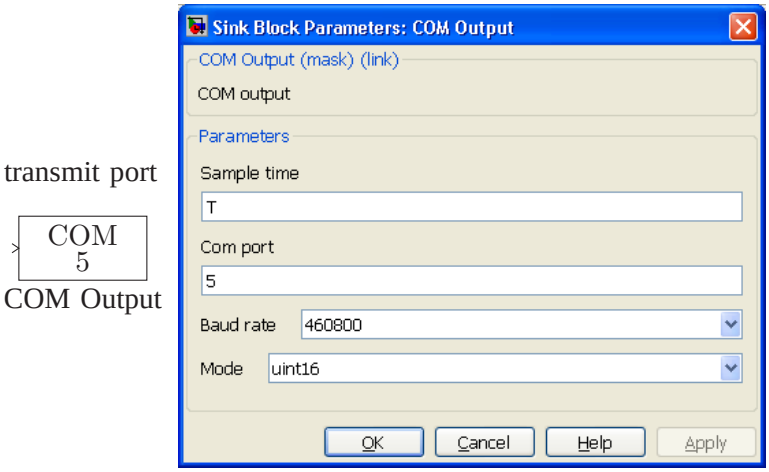
uint16 mode $\Rightarrow$ $v = \text{uint16}(u)$

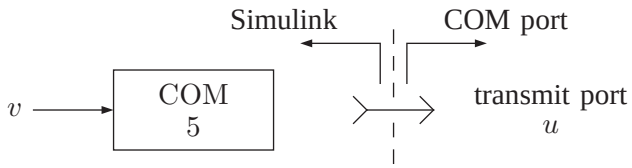
int8 mode $\Rightarrow$ $v = \text{int8}(u)$

uint8 mode $\Rightarrow$ $v = \text{uint8}(u)$

26. COM Output

- 256 COM output channels COM z (COM port) with transmit port $1 - 256$
- Block input: data to be written to transmit port
- COM output: data in float64, float32, int64, uint64, int32, uint32, int16, uint16, int8 or uint8 format





float64 mode $\Rightarrow$ $u = \text{float64}(v)$

float32 mode $\Rightarrow$ $u = \text{float32}(v)$

int64 mode $\Rightarrow$ $u = \text{int64}(v)$

uint64 mode $\Rightarrow$ $u = \text{uint64}(v)$

int32 mode $\Rightarrow$ $u = \text{int32}(v)$

uint32 mode $\Rightarrow$ $u = \text{uint32}(v)$

int16 mode $\Rightarrow$ $u = \text{int16}(v)$

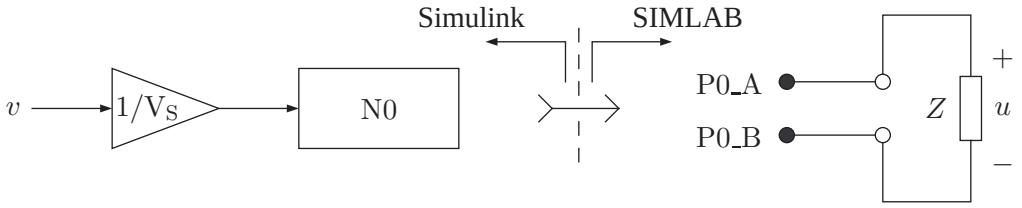
uint16 mode $\Rightarrow$ $u = \text{uint16}(v)$

int8 mode $\Rightarrow$ $u = \text{int8}(v)$

uint8 mode $\Rightarrow$ $u = \text{uint8}(v)$

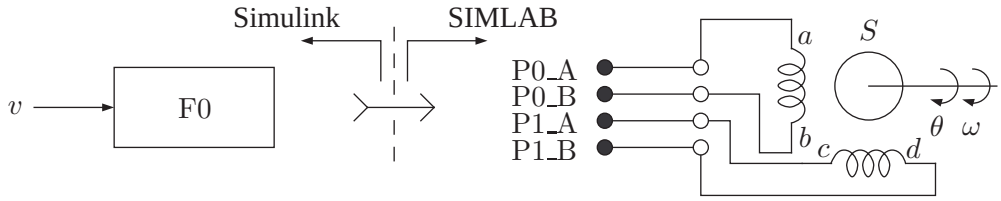
27. H-bridge Power Output

- 4 H-bridge power output channels P0_A, P0_B – P3_A, P3_B
- Board output: $0 - V_S$ V digital power signal (V_S is the power supply voltage)
- Capacity: 5 A
- H-bridge power outputs can be used as power amplifiers to drive heavy loads and stepper motors



$$\text{N0 in normal mode} \quad \Rightarrow \quad \text{lowpass equivalent of } u \approx \begin{cases} +V_S, & v \geq V_S \\ 2v - V_S, & 0 < v < V_S \\ -V_S, & v \leq 0 \end{cases}$$

$$\text{N0 in shifted mode} \quad \Rightarrow \quad \text{lowpass equivalent of } u \approx \begin{cases} +V_S, & v \geq +V_S \\ v, & -V_S < v < +V_S \\ -V_S, & v \leq -V_S \end{cases}$$

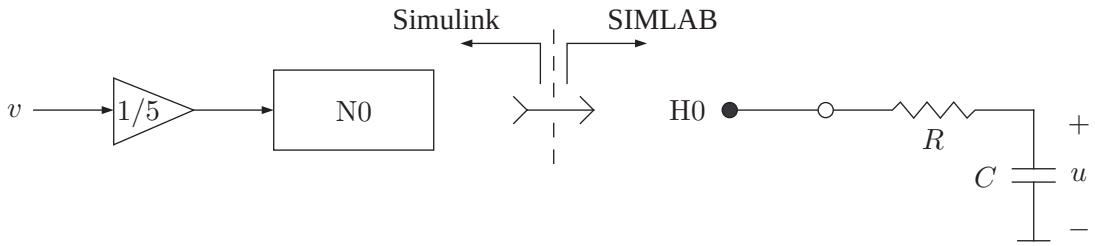


$$\text{F0 in position mode} \quad \Rightarrow \quad \theta \approx v$$

$$\text{F0 in velocity mode} \quad \Rightarrow \quad \omega \approx v$$

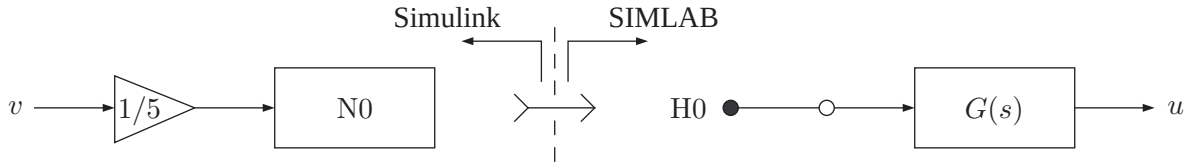
28. Pulse Filtering

- Lowpass filtered pulse outputs can be used as analog outputs
- Bandwidth of the lowpass filter should be sufficiently small (much smaller than the fundamental frequency of the pulse output)



$$\text{N0 in normal mode} \quad \Rightarrow \quad \text{lowpass equivalent of } u \approx \begin{cases} 5, & v \geq 5 \\ v, & 0 < v < 5 \\ 0, & v \leq 0 \end{cases}$$

$$\text{N0 in shifted mode} \quad \Rightarrow \quad \text{lowpass equivalent of } u \approx \begin{cases} 5, & v \geq +5 \\ v/2 + 5/2, & -5 < v < +5 \\ 0, & v \leq -5 \end{cases}$$

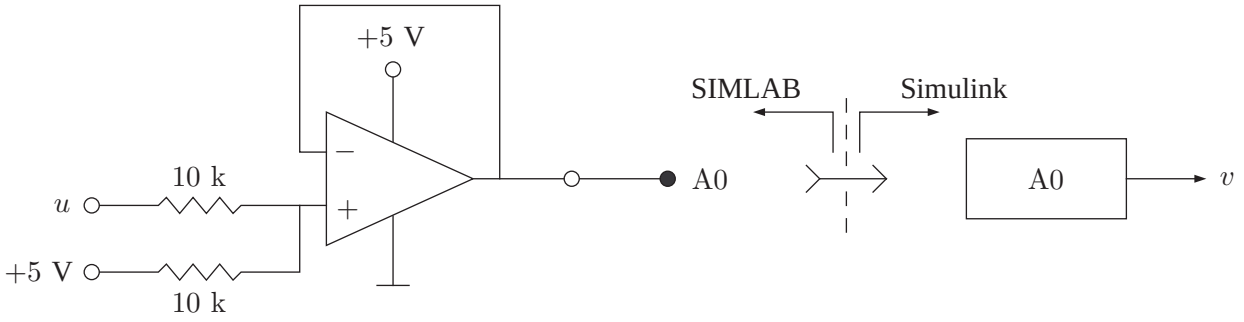


$$\text{N0 in normal mode} \quad \Rightarrow \quad \text{lowpass equivalent of } U(s) \approx G(s)V(s)$$

$$\text{N0 in shifted mode} \quad \Rightarrow \quad \text{lowpass equivalent of } U(s) \approx G(s)[V(s)/2 + 5/2/s]$$

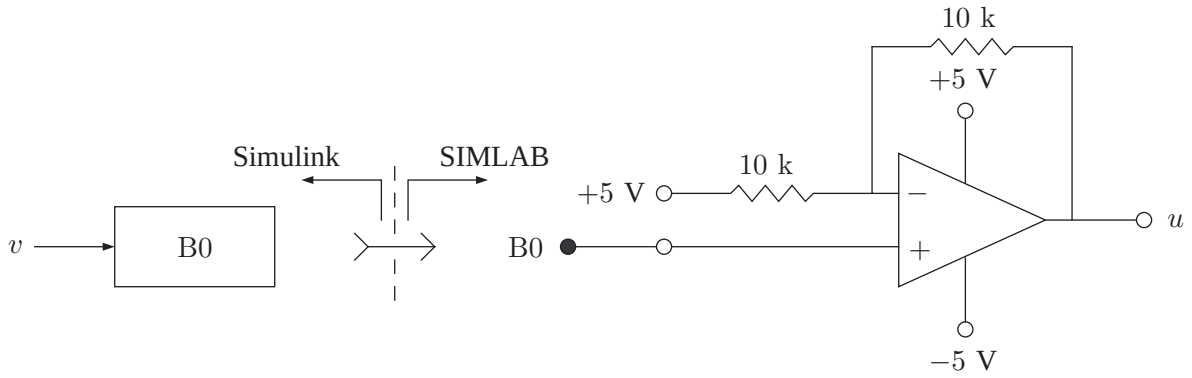
29. Level Conversion

- Negative voltage levels can not be applied directly to the analog inputs and negative voltage levels can not be obtained directly from the analog outputs
- Two simple level converter circuits to convert voltage levels are shown below



$$\text{A0 in unipolar mode} \quad \Rightarrow \quad v \approx \begin{cases} 5, & u \geq +5, \\ u/2 + 5/2, & -5 < u < +5, \\ 0, & u \leq -5 \end{cases}$$

$$\text{A0 in bipolar mode} \quad \Rightarrow \quad v \approx \begin{cases} +5, & u \geq +5, \\ u, & -5 < u < +5, \\ -5, & u \leq -5 \end{cases}$$



$$\text{B0 in unipolar mode} \quad \Rightarrow \quad u \approx \begin{cases} +5, & v \geq 5, \\ 2v - 5, & 0 < v < 5, \\ -5, & v \leq 0 \end{cases}$$

$$\text{B0 in bipolar mode} \quad \Rightarrow \quad u \approx \begin{cases} +5, & v \geq +5, \\ v, & -5 < v < +5, \\ -5, & v \leq -5 \end{cases}$$

30. Sampling Rate

- Serial link

$$\begin{array}{l}\text{number of input channels } n_i \leq 64\\ \text{number of output channels } n_o \leq 64\end{array} \quad \Rightarrow \quad \text{sampling rate } f = \frac{1}{T} \leq \frac{46080}{2\max(n_i, n_o) + 1}$$

- USB link

$$\begin{array}{l}\text{number of input channels } n_i \leq 64\\ \text{number of output channels } n_o \leq 64\end{array} \quad \Rightarrow \quad \text{sampling rate } f = \frac{1}{T} \leq 1024$$

- Wireless link

$$\begin{array}{l}\text{number of input channels } n_i \leq 64\\ \text{number of output channels } n_o \leq 64\end{array} \quad \Rightarrow \quad \text{sampling rate } f = \frac{1}{T} \leq \frac{11520}{2n_i + 2n_o + 7}$$

31. Usage

- Set up the real-time control board with the desired external connections and construct a Simulink model with the desired blocks.
- Define the sample time T ($T = 1/f$, where f is the sampling rate) and the stop time S at the command prompt in the Matlab command window.
- Build the Simulink model by clicking on "Tools $\rightarrow$ Code Generation $\rightarrow$ Build Model" or by pressing Ctrl+B.
- Click on the "Connect to target" button  to connect the board to the model and then click on the "Start real-time code" button  to run the model.
- Click on the "Stop real-time code" button  to stop the model or click on the "Disconnect from target" button  to disconnect the model from the board.
- If the real-time execution is terminated by clicking on the "Stop real-time code" button  , the model can be modified, rebuilt and rerun by following the above steps again.
- If, however, the real-time execution is terminated by clicking on the "Disconnect from target" button  , the board must be reset before rerunning the model even without any modification since the code is still running on the real-time board.
- Pressing the reset button on the board also stops the real-time execution when the board is used with the serial port.

32. Guidelines

- Refer to the examples that come with the platform for setting up the configuration parameters under "Simulation $\rightarrow$ Configuration Parameters..." for your model.
- Refer to the Matlab help files for setting up the configuration parameters under "Tools $\rightarrow$ External Mode Control Panel..." for your model.
- Refer to the Real-Time Windows Target help files for setting up the "Scope parameters" for external data collection.
- Confine all your project files to the SIMLAB installation folder and make sure that the "Current Folder" of Matlab is your SIMLAB installation folder.
- Make sure that the com port number of each SIMLAB block (default is 5) matches with the com port you are using.
- Rebuild your model whenever you make any changes in the parameters of the SIMLAB blocks in your model (even when Matlab does not warn you to do so).
- Fast pulse input can not be used together with pulse input, pulse output, fast pulse output, general pulse input and general pulse output in the same Simulink model.
- Fast pulse output can not be used together with pulse input, pulse output, fast pulse input, general pulse input and general pulse output in the same Simulink model.
- All relevant physical quantities (board and block inputs, outputs and parameters) cited in this document are in SI units for convenience.
- The given quantization and interpolation errors are based on the nominal values of components used on the SIMLAB board and are provided only for reference purpose (not guaranteed).
- Do not excessively load (actively or passively) the inputs and outputs of the board beyond their normal operating ranges.
- Refer to the data sheets of the components used on the board for their absolute maximum ratings and safe operating areas.

33. Applications

- Real-time signal analysis, synthesis, processing and visualization
- Parameter tuning and optimization
- Modeling, analysis and design of control systems
- Real-time control
- Hardware-in-the-loop simulation
- Real-time rapid control prototyping
- Teaching concepts and carrying out experiments in signals and systems labs
- Real-time data acquisition

34. Specifications

- Power supply: $6 - 15$ V, minimum 0.25 A, regulated
- Interface: UART (serial) link, USB link or wireless link
- Analog input: $\mathrm{A0} - \mathrm{A7}$, $0 - 5$ V analog, 12 bit resolution
- Analog output: $\mathrm{B0} - \mathrm{B7}$, $0 - 5$ V analog, 12 bit resolution
- Digital input: $\mathrm{C0}\ (\mathrm{c0} - \mathrm{c7})$, $0 - 5$ V digital, 8 lines
- Digital output: $\mathrm{D0}\ (\mathrm{d0} - \mathrm{d7})$, $0 - 5$ V digital, 8 lines
- Encoder input: $\mathrm{E0\_A}, \mathrm{E0\_B} - \mathrm{E3\_A}, \mathrm{E3\_B}$, $0 - 5$ V digital, 16 bit resolution
- Stepper output: $\mathrm{F0\_A}, \mathrm{F0\_B} - \mathrm{F3\_A}, \mathrm{F3\_B}$, $0 - 5$ V digital, 16 bit resolution
- Capture input: $\mathrm{G0} - \mathrm{G3}$, $0 - 5$ V digital, 16 bit resolution
- Frequency output: $\mathrm{H0} - \mathrm{H3}$, $0 - 5$ V digital, 16 bit resolution
- Sensor input: $\mathrm{I0} - \mathrm{I3}$, $0 - 5$ V digital, 16 bit resolution
- Servo output: $\mathrm{J0} - \mathrm{J3}$, $0 - 5$ V digital, 16 bit resolution
- Pulse input: $\mathrm{K0} - \mathrm{K3}$, $0 - 5$ V digital, 16 bit resolution
- Pulse output: $\mathrm{L0} - \mathrm{L3}$, $0 - 5$ V digital, 16 bit resolution
- Fast pulse input: $\mathrm{M0} - \mathrm{M3}$, $0 - 5$ V digital, 16 bit resolution
- Fast pulse output: $\mathrm{N0} - \mathrm{N3}$, $0 - 5$ V digital, 16 bit resolution
- General pulse input: $\mathrm{O0} - \mathrm{O3}$, $0 - 5$ V digital, 16 bit resolution
- General pulse output: $\mathrm{P0} - \mathrm{P3}$, $0 - 5$ V digital, 16 bit resolution
- Logic input: $\mathrm{Q0}$, $0 - 5$ V digital, 8 logic functions
- Logic output: $\mathrm{R0}$, $0 - 5$ V digital, 8 logic functions
- Counter input: $\mathrm{S0} - \mathrm{S3}$, $0 - 5$ V digital, 16 bit counter
- Timer output: $\mathrm{T0} - \mathrm{T3}$, $0 - 5$ V digital, 16 bit timer
- Test input: $\mathrm{U0} - \mathrm{U7}$ (used for test purpose)
- Test output: $\mathrm{V0} - \mathrm{V7}$ (used for test purpose)
- Reserved input: $\mathrm{W0} - \mathrm{W7}$ (reserved for future use)
- Reserved output: $\mathrm{X0} - \mathrm{X7}$ (reserved for future use)
- File input: LOG y.log, $8/64$ bit format
- File output: LOG z.log, $8/64$ bit format
- UDP input: UDP 127.0.0.1, $8/64$ bit format
- UDP output: UDP 127.0.0.1, $8/64$ bit format
- COM input: COM 5, $8/64$ bit format
- COM output: COM 5, $8/64$ bit format
- H-bridge: $\mathrm{P0\_A}, \mathrm{P0\_B} - \mathrm{P3\_A}, \mathrm{P3\_B}$, $0 -$ (supply voltage) V digital, 5 A
- Peripheral: WRT, IIC, SPI, CAN and DCI (optional)
- Regulator: VDD, 5 V, 0.25 A

- Ground: GND, 0 V
- Sampling rate: up to 15.2 kHz
- Size: 12.70 cm $\times$ 10.16 cm
- Weight: 72.5 g

35. Requirements

- PC with Windows XP or later and an expansion slot for a serial card or a USB port
- Matlab R2007b or later with Simulink, Real-Time Workshop (Matlab Coder and Simulink Coder) and Real-Time Windows Target (Simulink Desktop Real-Time)
- SIMLAB hardware (real-time control board) 1.1 or later
- SIMLAB software 1.1 or later
- Serial crossover cable or USB cable
- Power supply (regulated, $6 - 15$ V and at least 0.25 A)

36. Absolute Maximum Ratings

- Power supply voltage: minimum 3 V, maximum 16 V
- Each analog and digital input: minimum -0.3 V, maximum $+5.3$ V
- Each analog and digital output: minimum -25 mA, maximum $+25$ mA
- Each H-bridge power output: minimum -5 A, maximum $+5$ A
- Voltage regulator output: maximum 0.5 A (total)
- Total current from/into all inputs and outputs (except power supply, voltage regulator and H-bridges): minimum -200 mA, maximum $+200$ mA
- Operating ambient temperature: minimum 10 °C, maximum 50 °C